DisplayPort 1:2 Switch

FEATURES

- One Input Port to One of Two Output Ports
- Supports Data Rates up to 2.7Gbps
- Supports Dual-Mode DisplayPort
- Output Waveform Mimics Input Waveform Characteristics
- Enhanced ESD:
  - 12kV on all Main Link Pins
  - 10kV on all Auxiliary Pins
- Enhanced Commercial Temperature Range: 0°C to 85°C
- 56 Pin 8 × 8 QFN Package

APPLICATIONS

- Personal Computer Market
  - Desktop PC
  - Notebook PC
  - Docking Station
  - Standalone Video Card

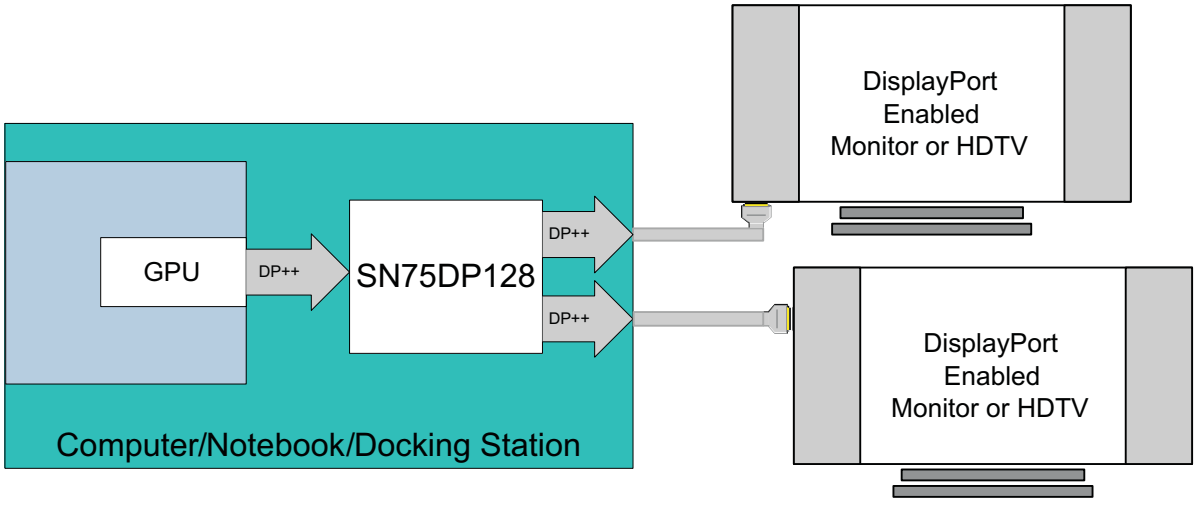
DESCRIPTION

The SN75DP128 is a one Dual-Mode DisplayPort input to one of two Dual-Mode DisplayPort outputs. The outputs will follow the input signal in a manner that provides the highest level of signal integrity while supporting the EMI benefits of spread spectrum clocking. Through the SN75DP128 data rates of up to 2.7Gbps through each link for a total throughput of up to 10.8Gbps can be realized.

In addition to the switching of the DisplayPort high speed signal lines, the SN75DP128 also supports the switching of the bi-directional auxiliary (AUX), Hot Plug Detect (HPD), and Cable Adapter Detect (CAD) channels. The Auxiliary differential pair supports Dual-Mode DisplayPort operation with the ability to be configured as a bi-directional differential bus while in DisplayPort mode or an I^{2}C™ bus while in TMDS mode

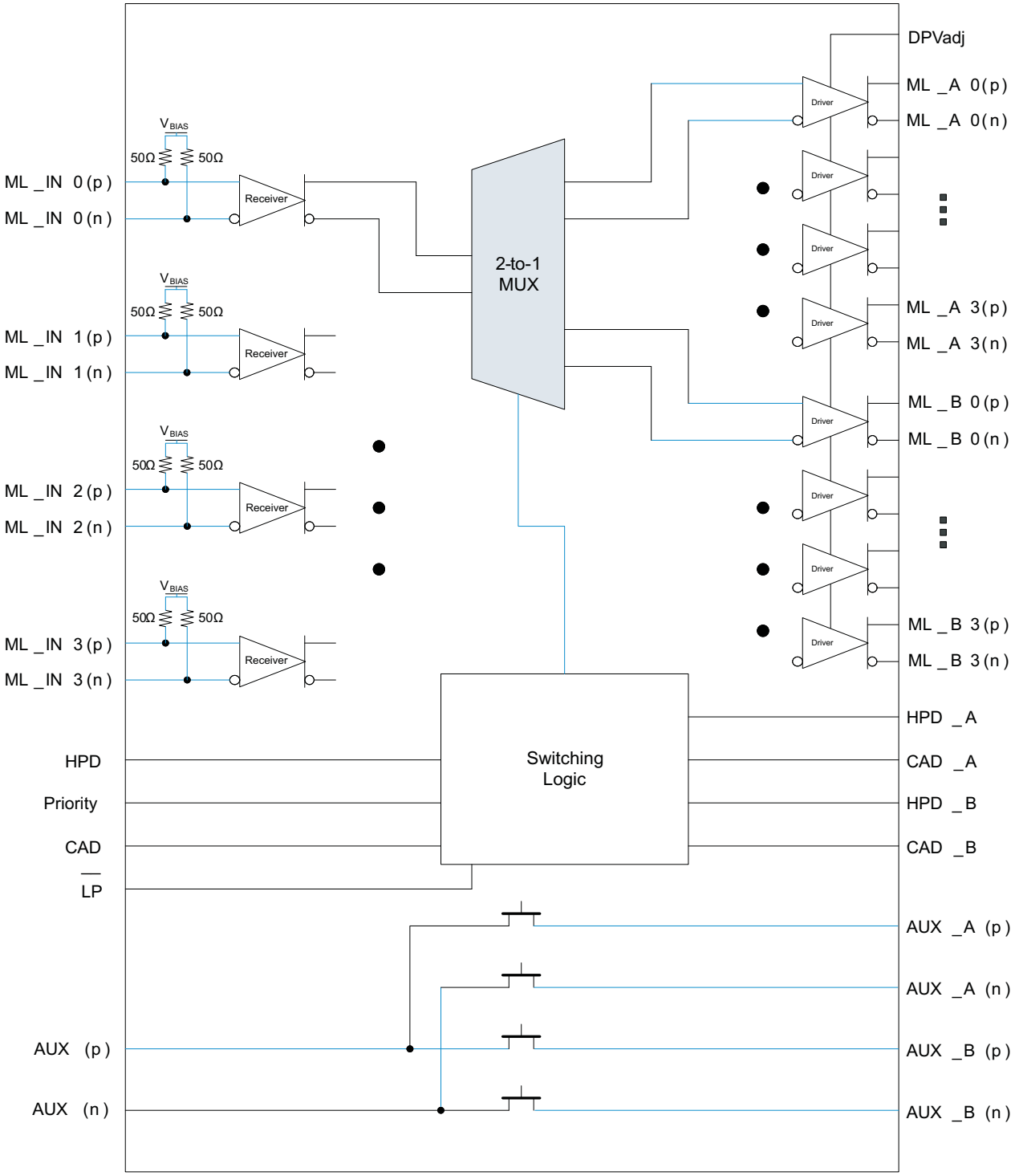
The SN75DP128 is characterized for operation over ambient air temperature of 0°C to 85°C.

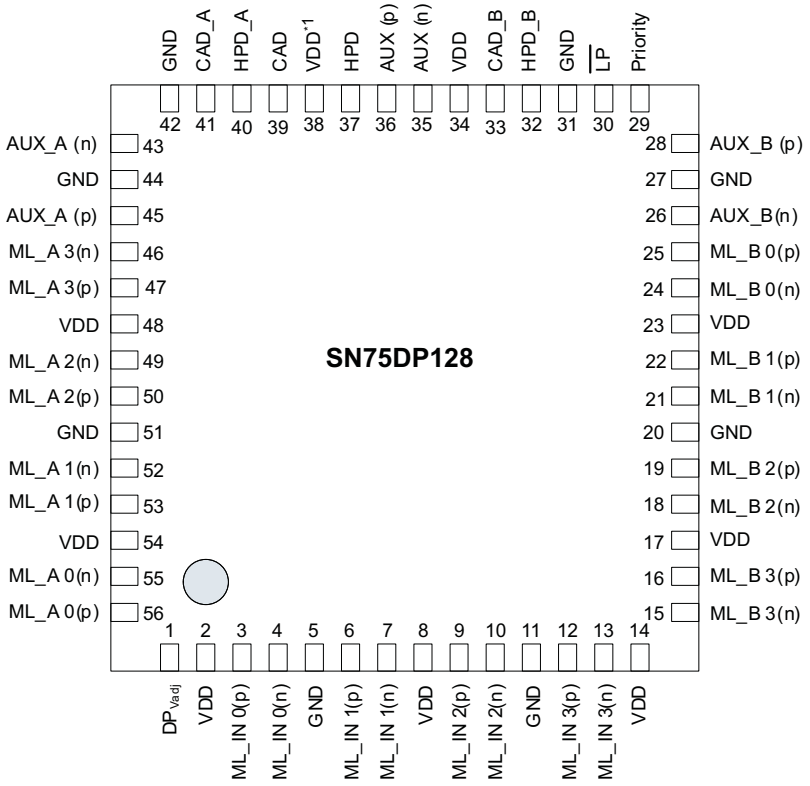
TYPICAL APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DATA FLOW BLOCK DIAGRAM





TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
MAIN LINK INPUT PINS			
ML_IN 0	3, 4	I	DisplayPort Main Link Channel 0 Differential Input
ML_IN 1	6, 7	I	DisplayPort Main Link Channel 1 Differential Input
ML_IN 2	9, 10	I	DisplayPort Main Link Channel 2 Differential Input
ML_IN 3	12, 13	I	DisplayPort Main Link Channel 3 Differential Input
MAIN LINK PORT A OUTPUT PINS			
ML_A 0	56, 55	O	DisplayPort Main Link Port A Channel 0 Differential Output
ML_A 1	53, 52	O	DisplayPort Main Link Port A Channel 1 Differential Output
ML_A 2	50, 49	O	DisplayPort Main Link Port A Channel 2 Differential Output
ML_A 3	47, 46	O	DisplayPort Main Link Port A Channel 3 Differential Output
MAIN LINK PORT B OUTPUT PINS			
ML_B 0	25, 24	O	DisplayPort Main Link Port B Channel 0 Differential Output
ML_B 1	22, 21	O	DisplayPort Main Link Port B Channel 1 Differential Output
ML_B 2	19, 18	O	DisplayPort Main Link Port B Channel 2 Differential Output
ML_B 3	16, 15	O	DisplayPort Main Link Port B Channel 3 Differential Output
HOT PLUG DETECT PINS			
HPD	37	O	Hot Plug Detect Output to the DisplayPort Source
HDP_A	40	I	Port A Hot Plug Detect Input
HPD_B	32	I	Port B hot Plug Detect Input
AUXILIARY DATA PINS			
AUX	36, 35	I/O	Source Side Bidirectional DisplayPort Auxiliary Data Line
AUX_A	45, 43	I/O	Port A Bidirectional DisplayPort Auxiliary Data Line

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AUX_B	28, 26	I/O	Port B Bidirectional DisplayPort Auxiliary Data Line
CABLE ADAPTER DETECT PINS			
CAD	39	O	Cable Adapter Detect Output to the DisplayPort Source
CAD_A	41	I	Port A Cable Adapter Detect Input
CAD_B	33	I	Port B Cable Adapter Detect Input
CONTROL PINS			
$\overline{LP}$	30	I	Low Power Select Bar
Priority	29	I	Output Port Priority selection
DPVadj	1	I	DisplayPort Main Link Output Gain Adjustment
SUPPLY and GROUND PINS			
VDD	2, 8, 14, 17, 23, 34, 48, 54		Primary Supply Voltage
VDD[*1]	38		HPD and CAD Output Voltage
GND	5, 11, 20, 27, 42, 44, 51		Ground

Table 1. Control Pin Lookup Table

SIGNAL	LEVEL[(1)]	STATE	DESCRIPTION
$\overline{LP}$	H	Normal Mode	Normal operational mode for device
	L	Low Power Mode	Device is forced into a Low Power state causing the outputs to go to a high impedance state. All other inputs are ignored
Priority	H	Port B has Priority	If both HPD_A and HPD_B are high, Port B will be selected
	L	Port A has Priority	If both HPD_A and HPD_B are high, Port A will be selected
DP_{Vadj}	4.53 kΩ	Increased Gain	Main Link DisplayPort Output will have an increased voltage swing
	6.49 kΩ	Normal Gain	Main Link DisplayPort Output will have a nominal voltage swing
	10 kΩ	Decreased Gain	Main Link DisplayPort Output will have a decreased voltage swing

(1) (H) Logic High; (L) Logic Low

Explanation of the internal switching logic of the SN75DP128 is located in the Application Information section at the end of the data sheet.

ORDERING INFORMATION[(1)]

PART NUMBER	PART MARKING	PACKAGE
SN75DP128RTQR	DP128	56-pin QFN Reel (large)
SN75DP128RTQT	DP128	56-pin QFN Reel (small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
Supply Voltage Range(2)	V_{DD}, V_{DD}*1		–0.3 to 5.25	V
Voltage Range	Main Link I/O (ML_IN x, ML_A x, ML_B x) Differential Voltage		1.5	V
	HPD and CAD I/O		–0.3 to VDD + 0.3	V
	Auxiliary I/O		–0.3 to VDD + 0.3	V
	Control I/O		–0.3 to VDD + 0.3	V
Electrostatic discharge	Human body model(3)	Auxiliary I/O (AUX +/-, AUX_A +/-, & AUX_B +/-)	±10000	V
		All Other Pins	±12000	
	Charged-device model(3)		±1000	V
	Machine model(4)		±200	V
Continuous power dissipation			See Dissipation Rating Table	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	$T_A \leq 25°C$	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
56-pin QFN (RTQ)	Low-K	3623 mW	36.23 mW/°C	1449 mW
	High-K	1109 mW	11.03 mW/°C	443.9 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	4x4 Thermal vias under powerpad		11.03		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			20.4		C/W
P_D	Device power dissipation DisplayPort selected	$\overline{LP}$ = 5V, ML: V_{ID} = 600 mV, 2.7 Gbps PRBS; AUX: V_{ID} = 500 mV, 1Mbps PRBS; HPD/CAD A and B = 5V; V_{DD}*1 = V_{DD}		300	340	mW
P_{SD}	Device power dissipation under low power	$\overline{LP}$ = 0V, HPD/CAD A and B = 5V; V_{DD}*1 = V_{DD}			85	µW

(1) The maximum rating is simulated under 5.25 V VDD.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Supply Voltage	4.5	5	5.25	V
V_{DD}*1	HPD and CAD Output reference voltage	1.62		5.25	V
T_A	Operating free-air temperature	0		85	°C
MAIN LINK DIFFERENTIAL PINS					
V_{ID}	Peak-to-peak input differential voltage	0.15		1.4	V
d_R	Data rate			2.7	Gbps
R_t	Termination resistance	45	50	55	Ω
V_{Oterm}	Output termination voltage	0		2	V
AUXILIARY PINS					

RECOMMENDED OPERATING CONDITIONS (continued)

		MIN	NOM	MAX	UNIT
V_I	Input voltage	0		3.6	V
d_R	Data rate			1	MHz
HPD, CAD, AND CONTROL PINS					
V_{IH}	High-level input voltage	2		5.25	V
V_{IL}	Low-level input voltage	0		0.8	V

DEVICE POWER

The SN75DP128 is designed to operate off a single 5V supply.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	LP = 5V, V_{DD}*1 = V_{DD} ML: V_{ID} = 600 mV, 2.7 Gbps PRBS AUX: V_{ID} = 500 mV, 1 Mbps PRBS HPD/CAD A and B = 5 V		60	65	mA
I_{DD}*1	Supply current	V_{DD}*1 = 5.25 V		0.1	4	mA
I_{SD}	Shutdown current	$\overline{LP}$ = 0 V		1	16	µA

HOT PLUG AND CABLE ADAPTER DETECT

The SN75DP128 is designed to support the switching of the Hot Plug Detect and Cable adapter Detect signals. The SN75DP128 has a built in level shifter for the HPD and CAD outputs. The output voltage level of the HPD and CAD pins is defined by the voltage level of the V_{DD}*1 pin. Explanation of HPD and the internal logic of the SN75DP128 is located in the application section at the end of the data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH5}	High-level output voltage	I_{OH} = –100 µA,	V_{DD}*1 = 5 V	4.5		5	V
$V_{OH3.3}$	High-level output voltage	I_{OH} = –100 µA,	V_{DD}*1 = 3.3 V	3		3.3	V
$V_{OH2.5}$	High-level output voltage	I_{OH} = –100 µA,	V_{DD}*1 = 2.5 V	2.25		2.5	V
$V_{OH1.8}$	High-level output voltage	I_{OH} = –100 µA,	V_{DD}*1 = 1.8 V	1.62		1.8	V
V_{OL}	Low-level output voltage	I_{OH} = 100 µA		0		0.4	V
I_H	High-level input current	V_{IH} = 2.0 V,	V_{DD} = 5.25 V	–10		10	µA
I_L	Low-level input current	V_{IL} = 0.8 V,	V_{DD} = 5.25 V	–10		10	µA

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD(CAD)}$	Propagation delay	V_{DD}*1 = 5 V	5		30	ns
$t_{PD(HPD)}$	Propagation delay	V_{DD}*1 = 5 V	30		110	ns
$t_{T1(HPD)}$	HPD logic switch pause time	V_{DD}*1 = 5 V	2		4.7	ms
$t_{T2(HPD)}$	HPD logic switch time	V_{DD}*1 = 5 V	170		400	ms
$t_{M(HPD)}$	Minimum output pulse duration	V_{DD}*1 = 5 V	100			ns
$t_{Z(HPD)}$	Low Power to High-level propagation delay	V_{DD}*1 = 5 V	30	50	110	ns

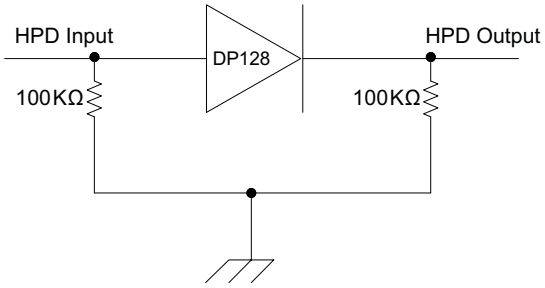


Figure 1. HPD Test Circuit

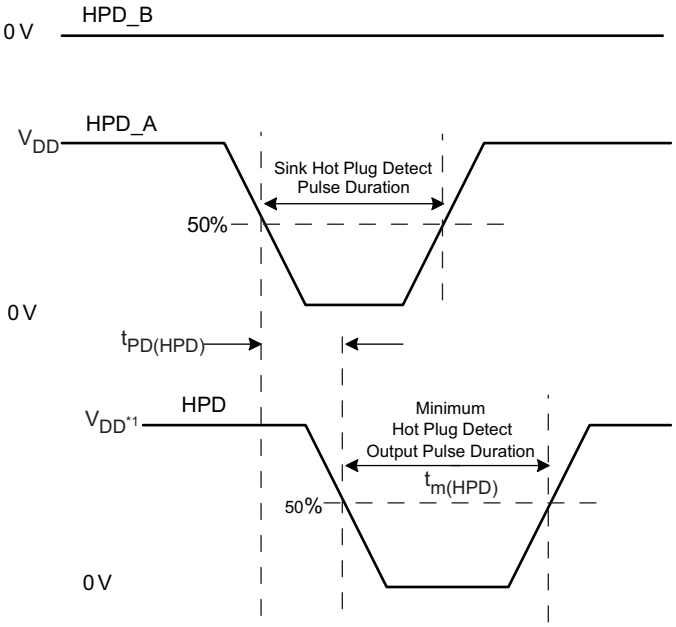


Figure 2. HPD Timing Diagram #1

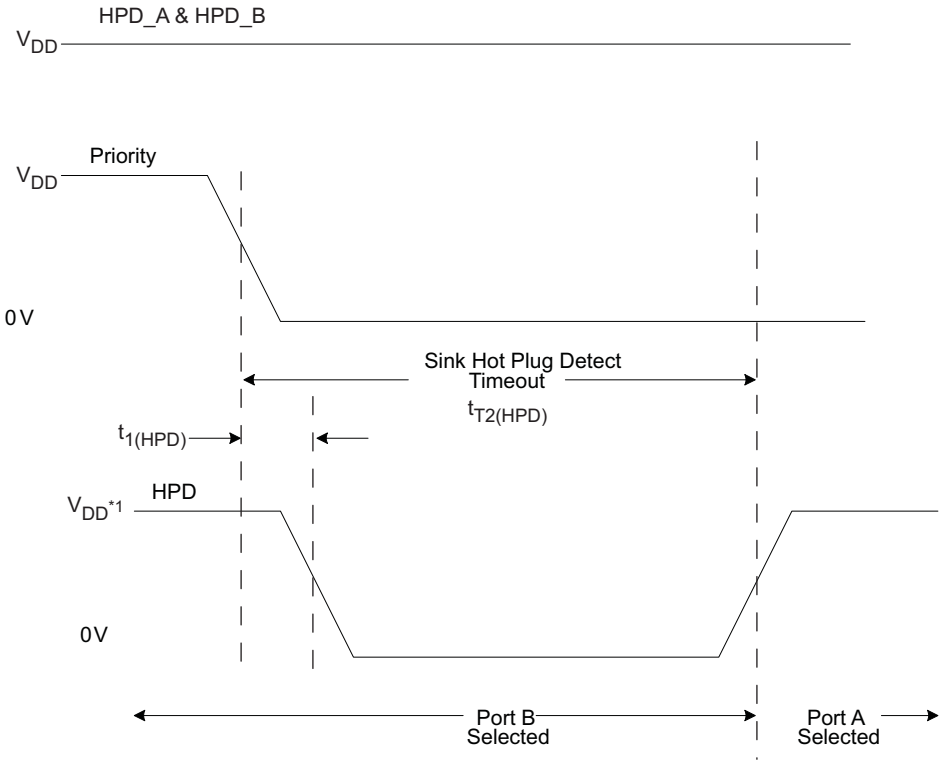


Figure 3. HPD Timing Diagram #2

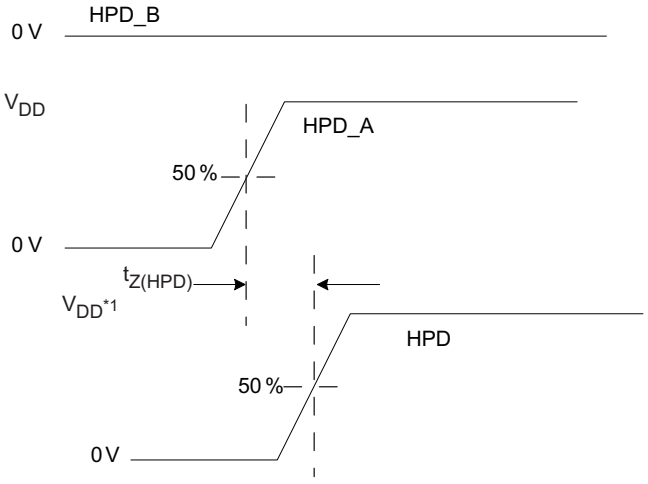


Figure 4. HPD Timing Diagram #3

Auxiliary Pins

The SN75DP128 is designed to support the 1:2 switching of the bidirectional auxiliary signals in both a differential (DisplayPort) mode and an I^2C (DVI, HDMI) mode. The performance of the Auxiliary bus is optimized based on the status of the selected output port's CAD pin.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{Pass1}	Maximum passthrough voltage (CAD=1)	V_{DD} = 4.5 V, V_I = 5 V, I_O = 100 µA	2.4		3.6	V
I_{OZ}	Output current from unselected output	V_{DD} = 5.25 V, V_O = 0–3.6 V, V_I = 0 V	–5		5	µA
$C_{IO(off)}$	I/O capacitance when in low power	DC bias = 1 V, AC = 1.4 Vp-p, F = 100 kHz,		9	12	pF
$C_{IO(on)}$	I/O capacitance when in normal operation	DC bias = 1 V, AC = 1.4 Vp-p, F = 100 kHz, CAD = High		18	25	pF
$r_{ON(C0)}$	On resistance	V_{DD} = 4.5 V, V_I = 0 – 3.6 V, I_O = 5 mA, CAD = Low		3.5	10	Ω
Δr_{ON}	On resistance	V_{DD} = 4.5 V, V_I = 0 – 3.6 V, I_O = 5 mA, CAD = Low		1	5	Ω
$r_{ON(C1)}$	On resistance	V_{DD} = 4.5 V, V_I = 0.4 V, I_O = 3 mA, CAD = High		10	18	Ω

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{sk(AUX)}$	Intra-pair skew	V_{ID} = 400 mV, V_{IC} = 2 V		40	80	ps
$I_{L(AUX)}$	Single Line Insertion Loss	V_{ID} = 500 mV, V_{IC} = 2 V, F = 1 MHz, CAD = Low			0.4	dB
$t_{PLH(AUXC0)}$	Propagation delay time, low to high	CAD = Low, F = 1 MHz			3	ps
$t_{PHL(AUXC0)}$	Propagation delay time, high to low	CAD = Low, F = 1 MHz			3	ps
$t_{PLH(AUXC1)}$	Propagation delay time, low to high	CAD = High, F = 100 kHz			3	ns
$t_{PHL(AUXC1)}$	Propagation delay time, high to low	CAD = High, F = 100 kHz			3	ns

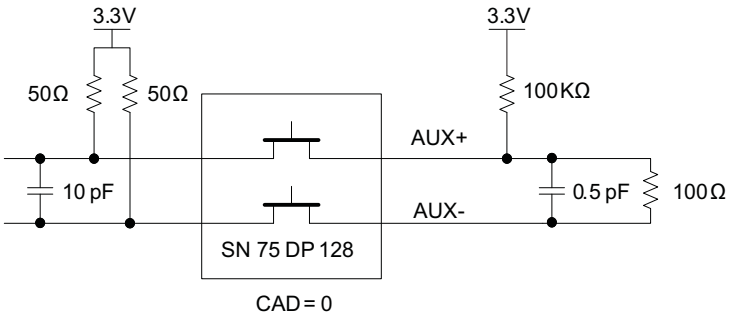


Figure 5. Auxiliary Channel Test Circuit (CAD = LOW)

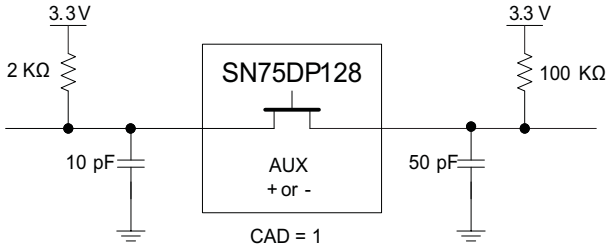


Figure 6. Auxiliary Channel Test Circuit (CAD = HIGH)

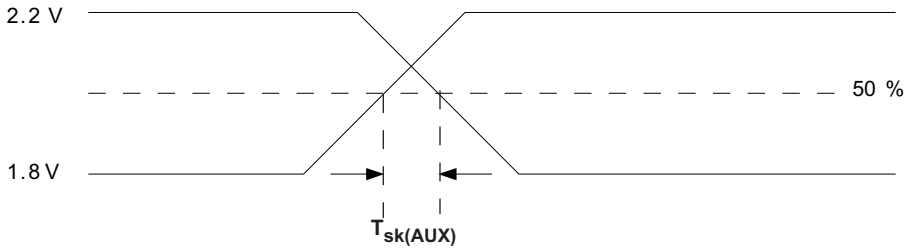


Figure 7. Auxiliary Channel Skew Measurement

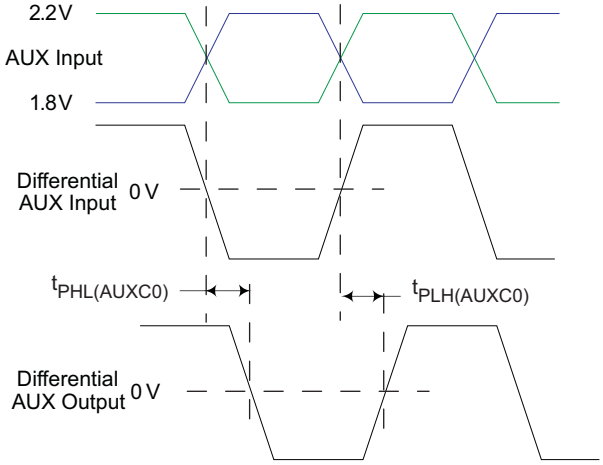


Figure 8. Auxiliary Channel Delay Measurement (CAD = LOW)

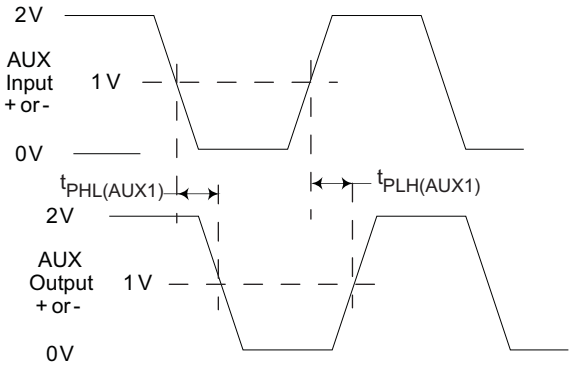


Figure 9. Auxiliary Channel Delay Measurement (CAD = HIGH)

Main Link Pins

The SN75DP128 is designed to support the 1:2 switching of DisplayPort's high speed differential main link. The main link I/O of the SN75DP128 are designed to track the magnitude and frequency characteristics of the input waveform and replicate them on the output. A feature has also been incorporated in the SN75DP128 to either increase or decrease the output amplitude via the resistor connected between the DPVADJ pin and ground.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{I/O(2)}$	Difference between input and output) voltages ($V_{OD} - V_{ID}$)	V_{ID} = 200 mV, DPV_{adj} = 6.5 kΩ	0	30	60	mV
$\Delta V_{I/O(3)}$		V_{ID} = 300 mV, DPV_{adj} = 6.5 kΩ	–24	11	36	mV
$\Delta V_{I/O(4)}$		V_{ID} = 400 mV, DPV_{adj} = 6.5 kΩ	–45	–15	15	mV
$\Delta V_{I/O(6)}$		V_{ID} = 600 mV, DPV_{adj} = 6.5 kΩ	–87	–47	–22	mV
R_{INT}	Input termination impedance		45	50	55	Ω
V_{Iterm}	Input termination voltage		0		2	V

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{R/F(DP)}$	Output edge rate (20%–80%)	Input edge rate = 80 ps (20%–80%)		115	160	ps
t_{PD}	Propagation delay time	F= 1 MHz, V_{ID} = 400 mV	200	240	280	ps
$t_{SK(1)}$	Intra-pair skew	F= 1 MHz, V_{ID} = 400 mV			20	ps
$t_{SK(2)}$	Inter-pair skew	F= 1 MHz, V_{ID} = 400 mV			40	ps
$t_{DPJIT(PP)}$	Peak-to-peak output residual jitter	d_R = 2.7 Gbps, V_{ID} = 400 mV, PRBS 27-1		25	35	ps

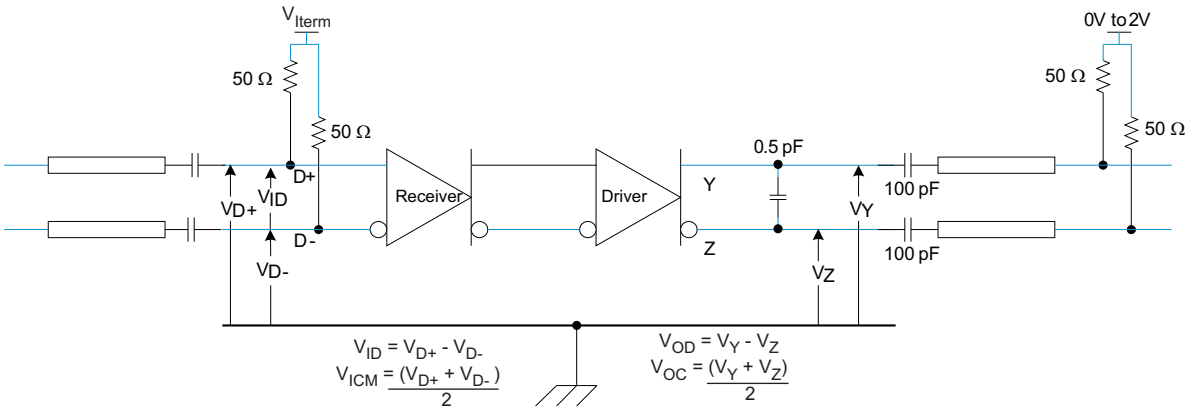


Figure 10. Main Link Test Circuit

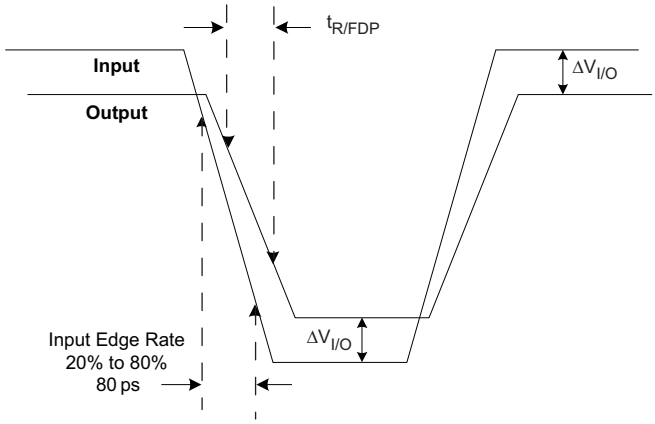


Figure 11. Main Link $\Delta V_{I/O}$ and Edge Rate Measurements

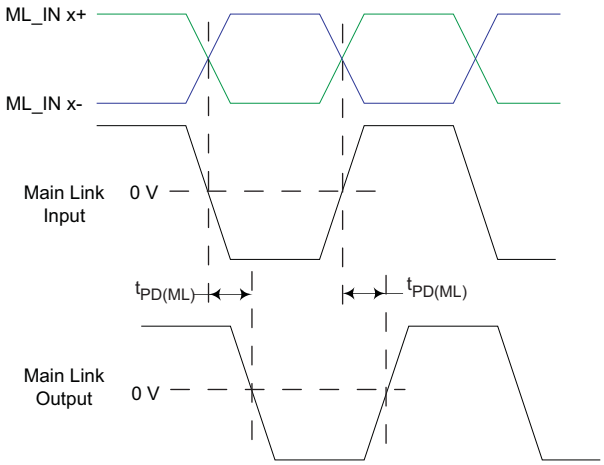


Figure 12. Main Link Delay Measurements

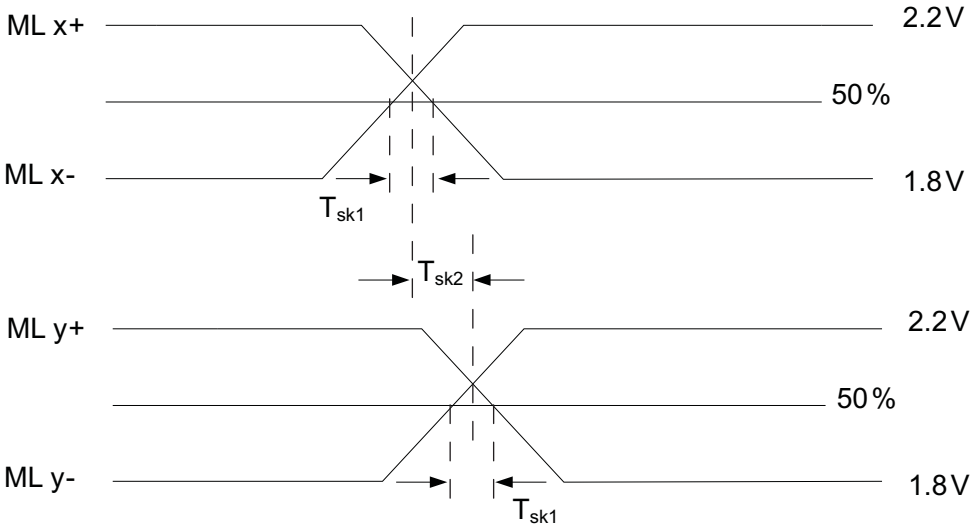


Figure 13. Main Link Skew Measurements

TYPICAL CHARACTERISTICS

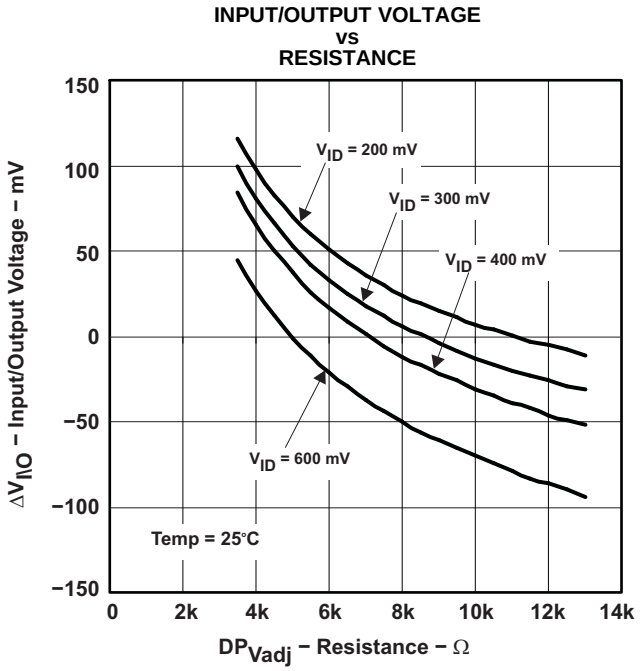


Figure 14.

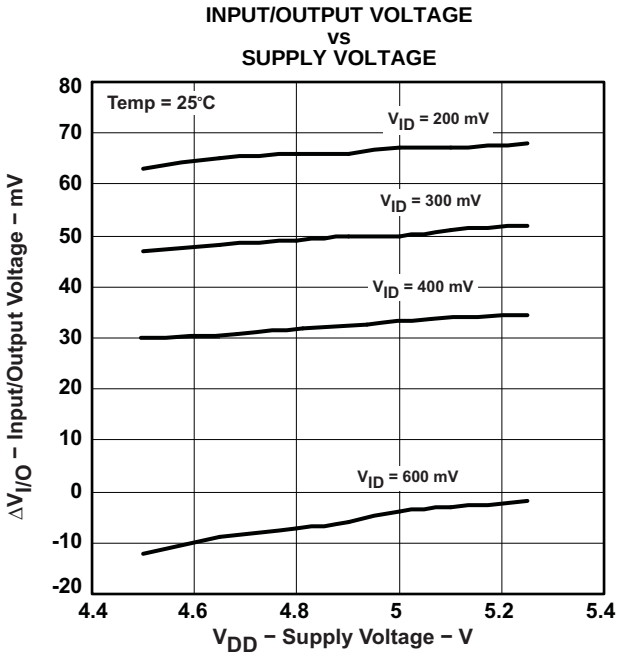


Figure 15.

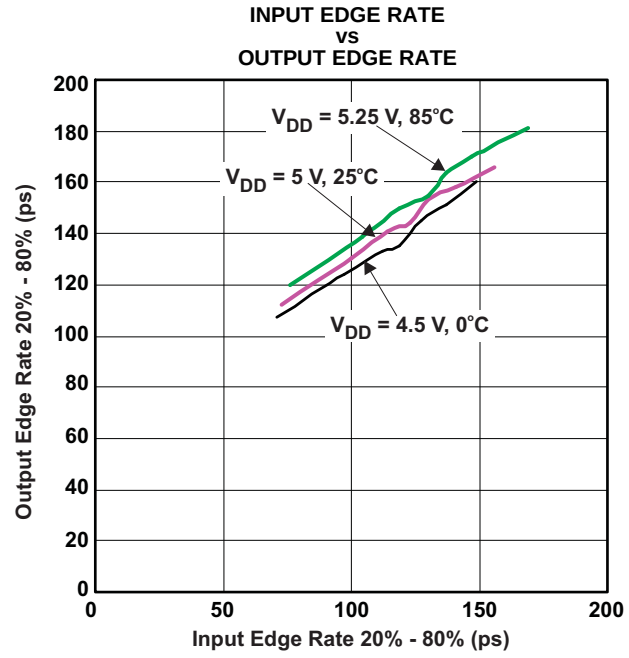


Figure 16.

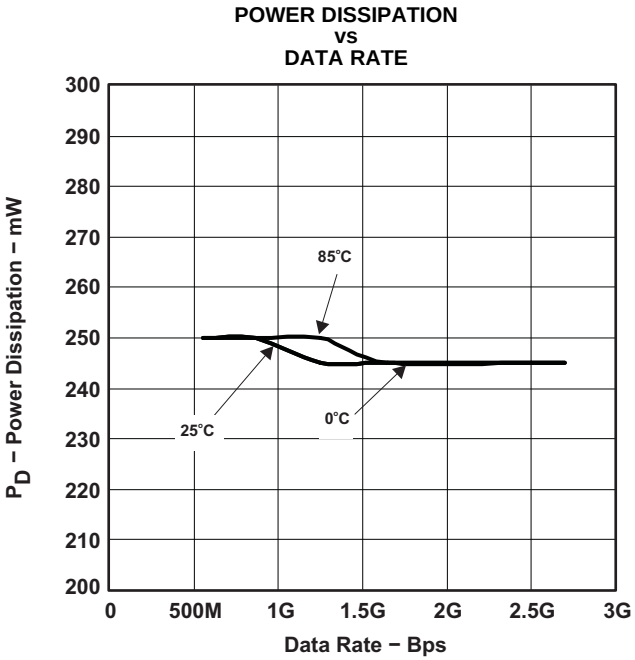


Figure 17.

APPLICATION INFORMATION

SWITCHING LOGIC

The switching logic of the SN75DP128 is tied to the state of the HPD input pins as well as the priority pin and low power pin. When both HPD_A and HPD_B input pins are LOW, the SN75DP128 enters the low power state. In this state the outputs are high impedance, and the device is shutdown to optimize power conservation. When either HPD_A or HPD_B goes high, the device enters the normal operational state, and the port associated with the HPD pin that went high is selected. If both HPD_A and HPD_B are HIGH, the port selection is determined by the state of the priority pin.

Several key factors were taken into consideration with this digital logic implementation of channel selection as well as HPD repeating. This logic has been divided into the following four scenarios.

1. Low power state to active state. There are two possible cases for this scenario depending on the state of the low power pin:
   - Case one: In this case both HPD inputs are initially LOW and the low power pin is also LOW. In this initial state the device is in a low power mode. Once one of the HPD inputs goes to a HIGH state, the device remains in the low power mode with both the main link and auxiliary I/O in a high impedance state. However, the port associated with the HPD input that went HIGH is still selected and the HPD output to the source is enabled and follows the logic state of the input HPD (see Figure 18). The state of the Priority pin has no effect in this scenario as only one HPD input port is active.

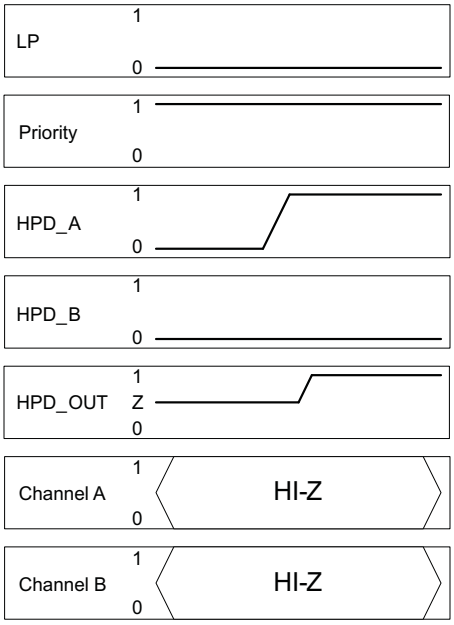


Figure 18.

   - Case two: In this case both HPD inputs are initially LOW and the low power pin is HIGH. In this initial state the device is in a low power mode. Once one of the HPD inputs goes to a HIGH state, the device comes out of the low power mode and enters active mode enabling the main link and auxiliary I/O. The port associated with the HPD input that went HIGH is selected and the HPD output to the source is enabled and follows the logic state of the input HPD (see Figure 19). This is specified as $t_{Z(HPD)}$. Again,the state of the Priority pin has no effect in this scenario as only one HPD input port is active.

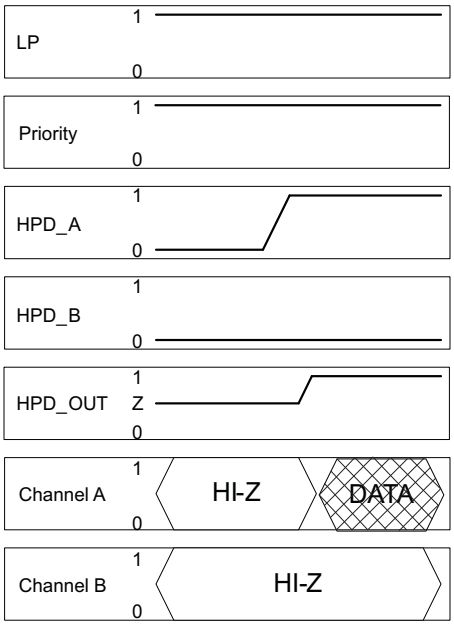


Figure 19.

2. HPD Changes on the selected port. There are also two possible starting cases for this scenario:
   – Case one: In this case only one HPD input is initially HIGH. The HPD output logic state follows the state of the HPD input. If the HPD input pulses LOW, as may be the case if the Sink device is requesting an interrupt, the HPD output to the source also pulses LOW for the same duration of time with a slight delay (see Figure 20). The delay of this signal through the SN75DP128 is specified as $t_{PD(HPD)}$. If the duration of the LOW pulse is less then $t_{M(HPD)}$, it may not be accurately repeated to the source. If the duration of the LOW pulse exceeds $t_{T2(HPD)}$, the device assumes that an unplug event has occurred and enters the low power state (see Figure 21). Once the HPD input goes high again, the device returns to the active state as indicated in scenario 1. The state of the Priority pin has no effect in this scenario as only one HPD input port is active.

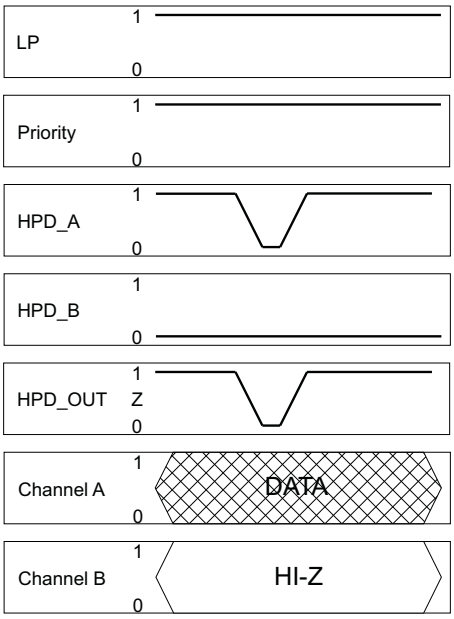


Figure 20.

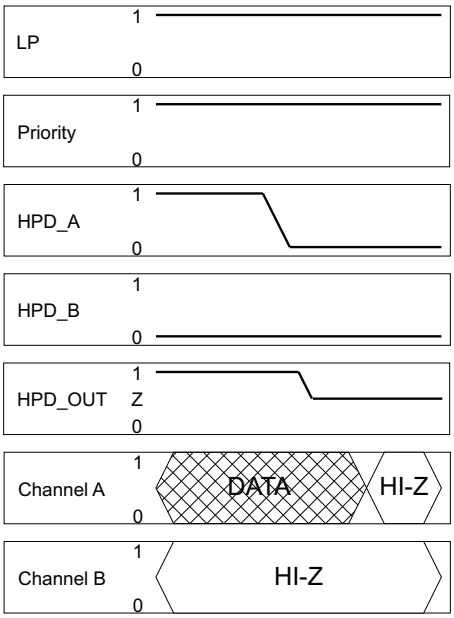


Figure 21.

– Case two: In this case both HPD inputs are initially HIGH and the selected port has been determined by the state of the priority pin. The HPD output logic state follows the state of the selected HPD input. If the HPD input pulses LOW, the HPD output to the source also pulses LOW for the same duration of time, again with a slight delay (see Figure 22). If the duration of the LOW pulse exceeds $t_{T2(HPD)}$, the device assumes that an unplug event has occurred and the other port is selected (see Figure 23). The case in which the previously selected port with priority goes high again is covered in scenario 3.

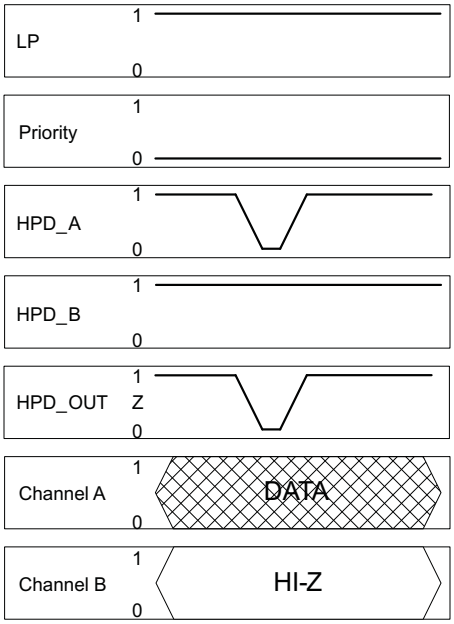


Figure 22.

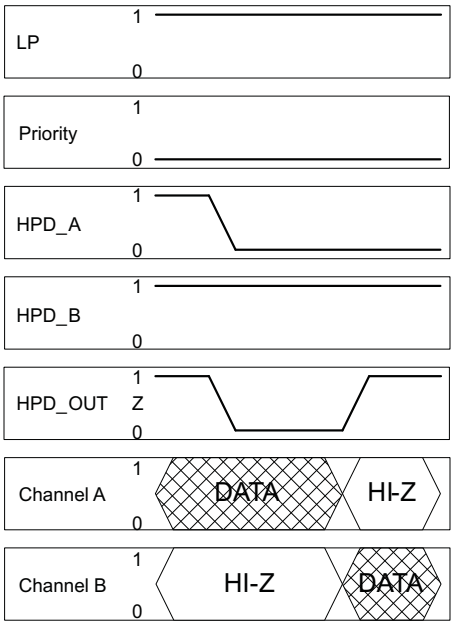


Figure 23.

3. One channel becomes active while other channel is already selected. There are also two possible starting cases for this scenario:
   – Case one: In this case the HPD input that is initially HIGH is from the port that has priority. Since the port with priority is already selected, any activity on the HPD input from the other port doesnot have any effect on the switch whatsoever (see Figure 24).

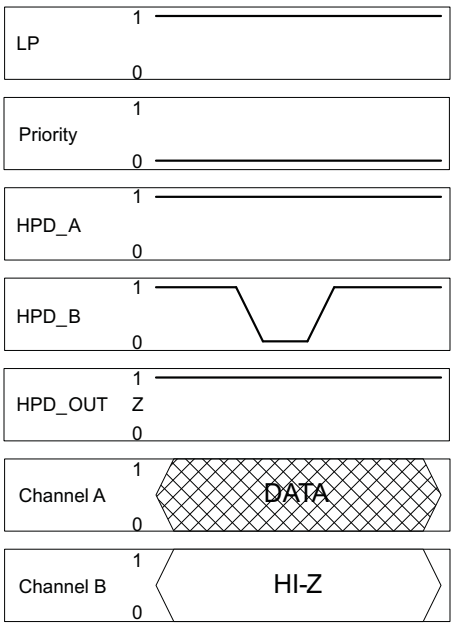


Figure 24.

   – Case two: In this case the HPD input that is initially HIGH is not the port with priority. When the HPD input of the port that has priority goes high, the HPD output is forced LOW for some time in order to simulate an unplug event to the source device. The duration of this LOW output is defined as $t_{T2(HPD)}$. If the HPD input of the port with priority pulses LOW for a short duration while the $t_{T2(HPD)}$ timer is counting down, the timer is reset. Once this time has passed the switch switches to the port with priority and the output HPD

once again follows the state of the newly selected channel's HPD input (see Figure 25).

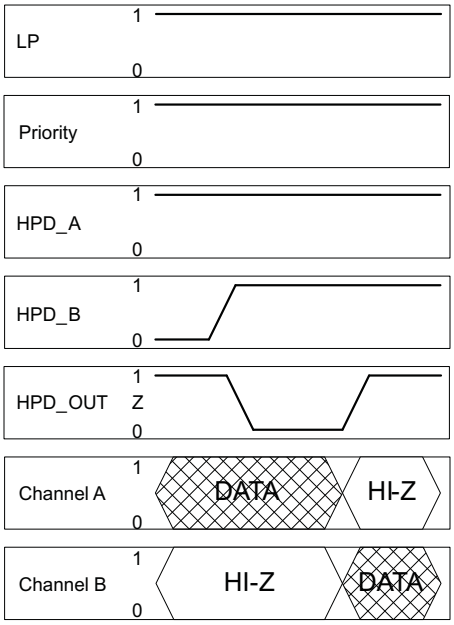


Figure 25.

4. 4. Priority pin is toggled. There are also two possible starting cases for this scenario:
   – Case one: In this case only one HPD input is HIGH. A port whose HPD input is LOW cannot be selected. In this case, the state of the priority pin has no effect on the switch (see Figure 26).

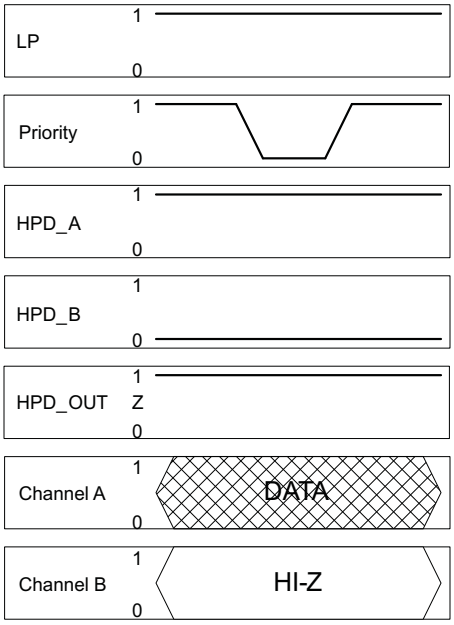


Figure 26.

   – Case two: In this case both HPD inputs are HIGH. Changing the state of the priority pin when both HPD inputs are high forces the device to switch which channel is selected. When a state change is detected on the priority pin, the device waits for a short period of time $t_{T1(HPD)}$ before responding (see Figure 27). The purpose for this pause is to allow for the priority signal to settle and also to allow the device to ignore potential glitches on the priority pin. Once $t_{T1(HPD)}$ has expired, the HPD output is forced LOW for $t_{T2(HPD)}$ and the device follows the chain of events outlined in scenario 3 case 2.

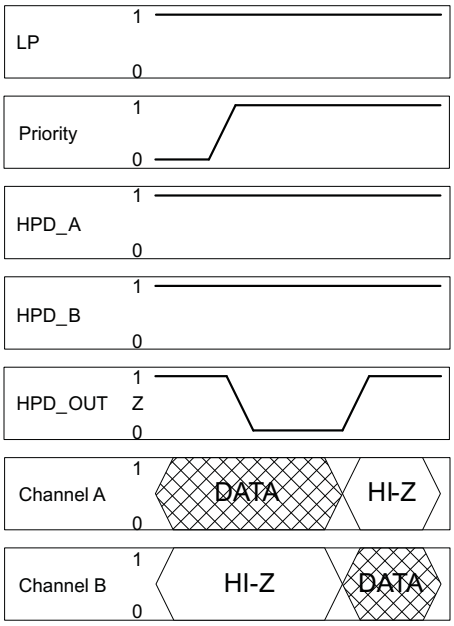

LP
1
0
Priority
1
0
HPD_A
1
0
HPD_B
1
0
HPD_OUT
1
Z
0
Channel A
1
DATA
HI-Z
0
Channel B
1
HI-Z
DATA
0

Figure 27.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN75DP128RTQR	ACTIVE	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN75DP128RTQRG4	ACTIVE	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN75DP128RTQT	ACTIVE	QFN	RTQ	56	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN75DP128RTQTG4	ACTIVE	QFN	RTQ	56	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

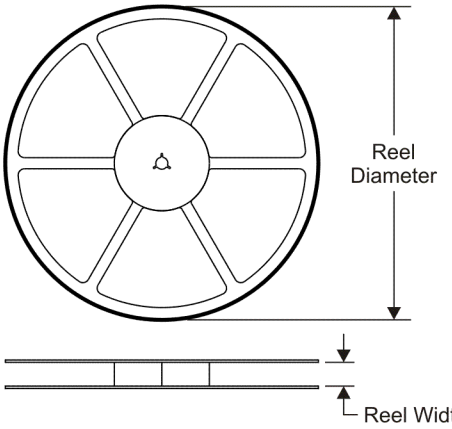
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

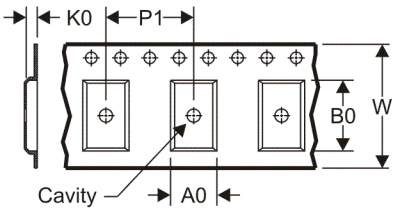
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

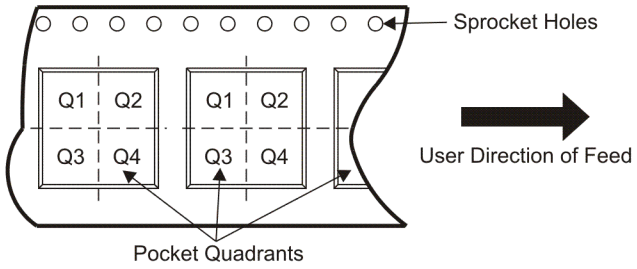


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

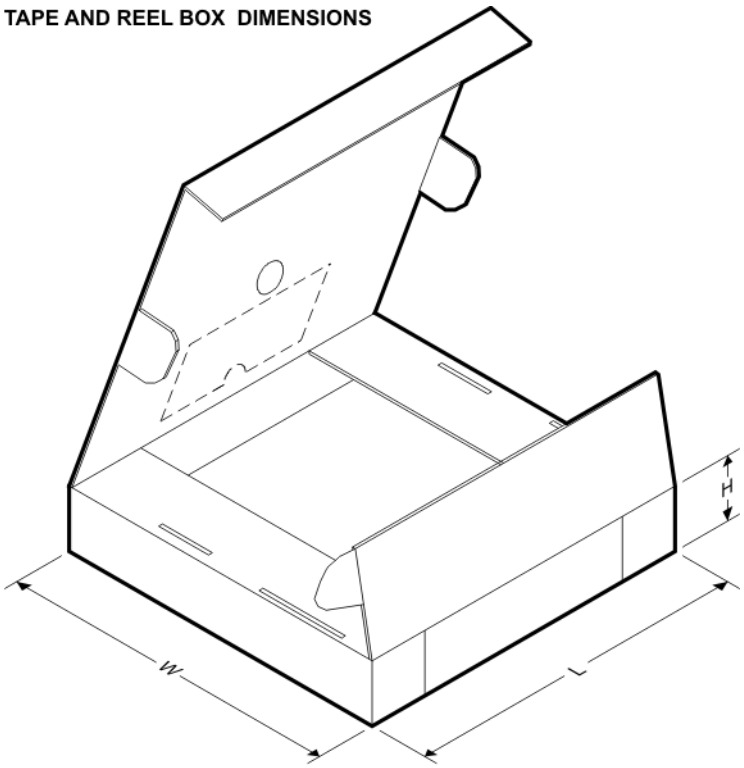
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP128RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
SN75DP128RTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2

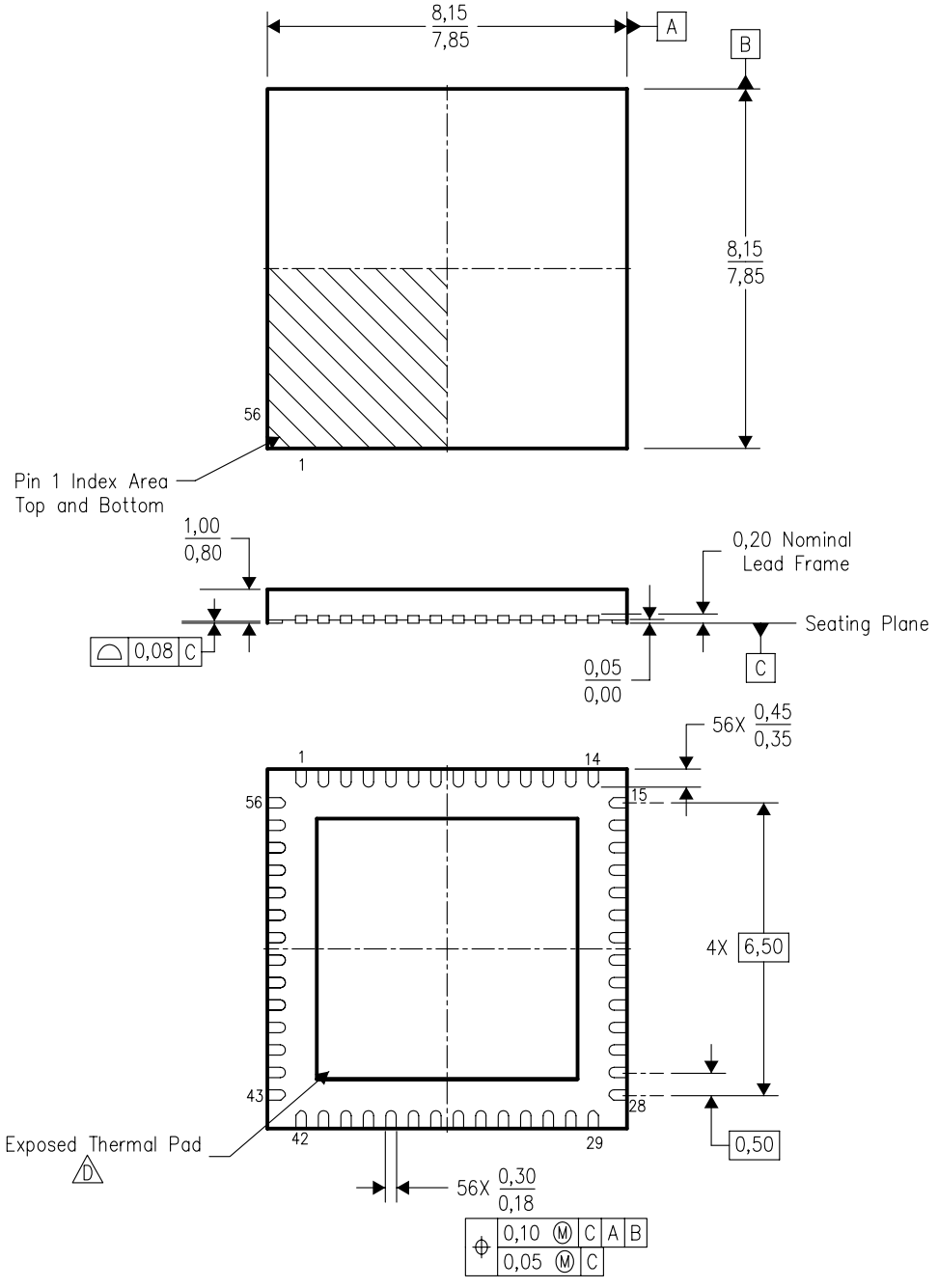
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP128RTQR	QFN	RTQ	56	2000	346.0	346.0	33.0
SN75DP128RTQT	QFN	RTQ	56	250	190.5	212.7	31.8

RTQ (S–PQFP–N56) PLASTIC QUAD FLATPACK



4206089/A 07/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

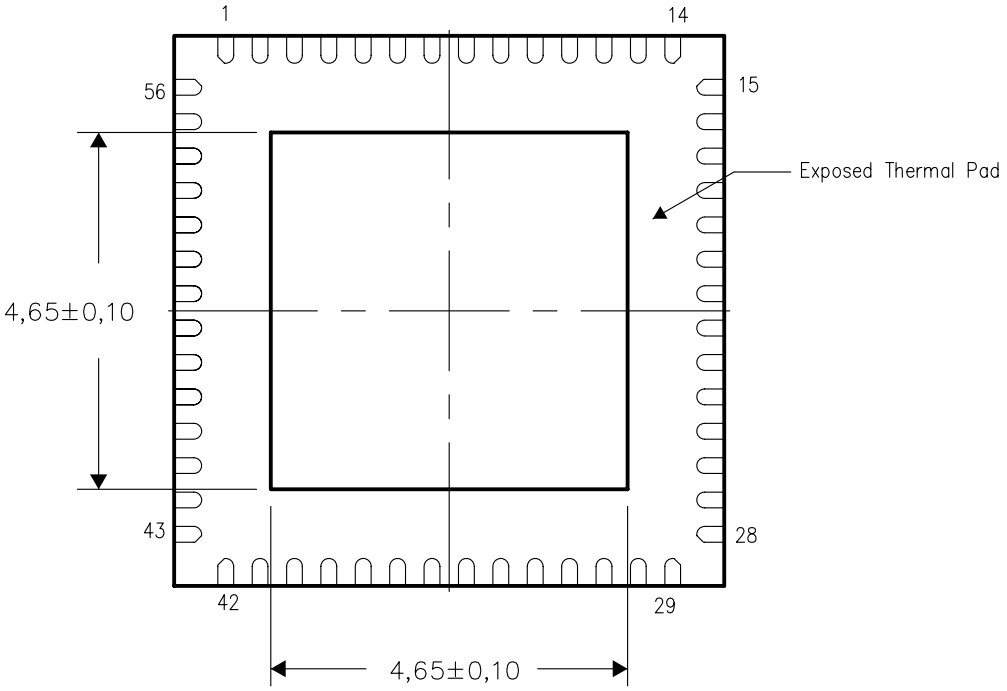
RTQ (S–PQFP–N56)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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